IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-22 (canceled).

23. (new) A semiconductor chip in which information of two values correspond to two different voltages comprising:

an information processing device;

an information memory device;

an encryption device;

a decryption device; and

a data bus,

wherein data is transferred from the information processing device to the information memory device through the data bus and stored in the information memory device after the data has been encrypted by the encryption device, and

wherein data read from the information memory device is input into the information processing device through the data bus after the data has been decrypted by the decryption device.

24. (new) The semiconductor chip according to claim 23, wherein the encryption performed by the encryption device is an exclusive OR operation of the data output from the information processing device and key data, and

wherein the decryption performed by the decryption device is exclusive OR operation by the data read from the information memory device and a key data.

25. (new) The semiconductor chip according to claim 23, wherein the encryption performed by the encryption device is an exclusive OR operation of the data output from the information processing device and key data appended to part of destination address data of the data in the information memory device; and

wherein the decryption performed by the decryption device is an exclusive OR operation of the data read from the information memory device and key data appended to a part of source address data of the data in the information memory device.

26. (new) The semiconductor chip according to claim 24, further comprising:

a random number generator,

wherein the key data is a random number generated by the random number generator.

27. (new) The semiconductor chip according to claim 24, further comprising:

a key buffer which is writable from the information processing device,

wherein the key buffer stores the key data transferred from the information processing device.

28. (new) The semiconductor chip according to claim 23, wherein the encryption device determines whether to encrypt the data output from the information processing device according to the destination address of the data in the information memory device, and

wherein the decryption device determines whether to decrypt the data read from the information memory device according to the source address of the data in the information memory device.

29. (new) The semiconductor chip according to claim 23, wherein the encryption device determines whether to encrypt the data output from the information processing device according to a data pattern, and

wherein the decryption device determines whether to decrypt the data read from the information memory device unit according to data pattern.

30. (new) A semiconductor chip in which information of two values corresponds to two different voltages comprising:

an information processing device;

an information memory device;

a first encryption device;

a second decryption device;

a first decryption device;

a second decryption device; and

a data bus,

wherein data output from the information processing device is encrypted by the first encryption device and output to the data bus,

wherein the data encrypted by the first encryption device is transferred to the first decryption device through the data bus, decrypted by the first decryption device and stored in the memory device,

wherein the data read from the information memory device is encrypted by the second encryption device and output to the data bus, and

wherein the data encrypted by the second encryption device is transferred to the second decryption device through the data bus, decrypted by the second decryption device and input to the information processing device.

31. (new) The semiconductor chip according to claim 30, wherein the encryption performed by the first encryption device is an exclusive OR operation of the data output from the information processing device and key data,

wherein the encryption performed by the second encryption device is an exclusive OR operation of the data transferred from the first encryption device and the key data, and

wherein the decryption performed by the second decryption device is an exclusive OR operation of the data transferred from the second encryption device and the key data.

32. (new) The semiconductor chip according to claim 31, further comprising:

a random number generation,

wherein the key data is a random number generated by the random number generator.